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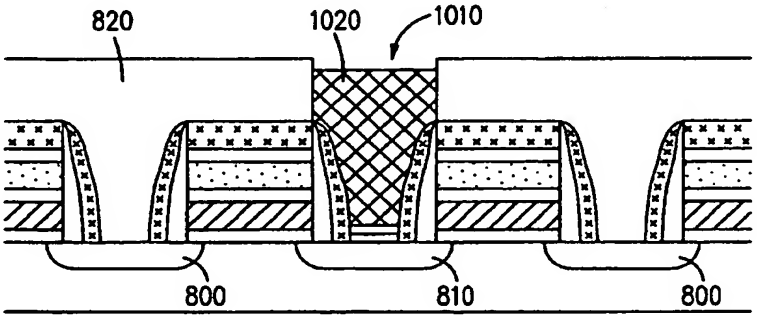
(54) Title: SELF-ALIGNED DRAIN CONTACT PMOS FLASH MEMORY AND PROCESS FOR MAKING SAME



(57) Abstract

A process and structure reduces the amount of dielectric, such as silicon dioxide, needed to separate polysilicon gates from drain contacts, thereby reducing the size of the individual memory cells and increasing the density of the associated memory array. Silicon nitride is formed on top and on the sides of the polysilicon gates prior to source and drain formation and self-aligned drain contact masking and etching. The presence of the silicon nitride spacers prevents the subsequent oxide etch, which forms the openings to the drain regions for the conducting drain contact, from removing polysilicon in the event of mask misalignment. Therefore, additional oxide, which was necessary to protect the polysilicon gates during the formation of the drain contact window when mask misalignment occurs, is no longer needed between the polysilicon gates and the drain contacts, resulting in higher density memory arrays.

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SELF-ALIGNED DRAIN CONTACT PMOS FLASH MEMORY AND PROCESS FOR MAKING SAME

BACKGROUND

Field of Invention

The present invention relates to methods for forming and connecting regions in a semiconductor device, and more particularly for connecting drain regions in P-channel flash memory cells to reduce memory array device sizes.

Related Art

A flash memory array comprises an array of flash memory cells. A prior art P channel flash EPROM cell 100 for use in such an array is shown in Figs. 1-3. In Fig. 1, a top view of memory cell 100 shows a drain contact 110, a P+ drain region 120, a floating gate 130, a control gate 140, field oxide regions 150a and 150b, and P+ source regions 160a and 160b, with source region 160a being the source of memory cell 100 and source region 160b being an extended portion of region 160a used to connect source regions of adjacent memory cells.

Fig. 2 is a cross sectional view of memory cell 100 along line A-A' of Fig. 1. P+ drain 120 and P+ source 160 are formed in an N well 200 with a channel formed therebetween. Floating gate 130 is insulated from the channel region by a tunnel oxide 210. Note that the term "tunnel oxide" is used to refer to what often is called "gate oxide" because in these kinds of memory devices, i.e., flash memory cells, the oxide under the gate must allow the tunneling of electrons

back and forth between the floating gate and the silicon substrate. The term "tunnel oxide" is used to reflect the dual function of the gate oxide (i.e., to insulate and to allow tunneling of electrons) in this type of memory. Above floating gate 130, an interpoly dielectric 220 provides insulation from control gate 140. A doped oxide 230 such as boron-phosphorous silicate glass (BPSG) or other suitable material insulates the underlying layers. Drain contact 110 includes a titanium nitride (TiN) layer 240 and a titanium (Ti) layer 250 located between drain 120 and a tungsten (W) plug 260. Fig. 3 is a cross sectional view of memory cell 100 along line B-B' of Fig. 1, showing field oxide 150 and tunnel oxide 210 separating N well 200 from floating gate 130, interpoly dielectric 220, and control gate 140.

In the design of a flash memory array, a primary goal is to increase the density, and thereby, for a given number of memory cells, decrease the size of the array. A typical approach to increasing the array density is to decrease the size of the individual cells 100 making up the memory array. One area of the cell 100 which has been difficult to reduce is the region between drain contact 110 and floating gate 130 and control gate 140, shown in Figs. 1 and 2. Reduction is difficult because of the need to protect gates 130 and 140 from being etched during the formation of drain contact 110. In forming drain contact 110, a masking operation first defines a contact region above drain 120. The unprotected areas of oxide layer 230 are then etched to expose the desired drain contact region. A tungsten plug 260 is then formed within this region, separated by a barrier layer of Ti 250 and TiN 240, to create drain contact 110. If the masking operation is misaligned such that areas over control gate 140 and/or floating gate 130 are unprotected, the subsequent

etching of oxide layer 230 will remove portions of these gates, thereby damaging cell 100. As a result, drain region 120 and the region of oxide 230 separating drain contact 110 from gates 130 and 140 must be larger than ideally necessary to insure that portions of gates 130 and 140 will not be etched away during formation of drain contact 110 if a masking misalignment occurs.

Accordingly, a flash memory cell is desired which has a decreased oxide separation between a drain contact and the floating and control gates, resulting in a smaller memory cell and thus a higher density memory array.

SUMMARY

According to the present invention, a process flow for forming self-aligned drain contacts in flash memory cells is provided which reduces the oxide separation between drain contacts and the floating and control gates. In one embodiment of this invention, a silicon dioxide layer and a nitride layer are formed on stacked-polysilicon floating and control gates and then etched to form oxide spacers and nitride spacers along the sidewalls of the stacked-gate structures. A dielectric such as BPSG or BPTEOS, deposited over the nitride spacers, the stacked-gate structures, and drain and source regions, is planarized for masking and etching. A drain contact mask exposes drain portions between nitride spacers, and the dielectric is etched to expose drain contact regions. Tungsten is deposited in these regions and etched back to form the drain contacts. Because the nitride layer around the polysilicon gates prevents polysilicon from being etched away during the oxide etch, additional oxide between the polysilicon gates and the drain contact is no longer needed to protect against the consequences of contact mask misalignment. As a result, the drain

contact can be much closer to the polysilicon gates, thereby reducing cell size and increasing memory array density.

The present invention will be more fully understood in light of the following detailed description taken together with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a top view of a conventional PMOS flash memory cell;

Fig. 2 is a cross sectional view of the memory cell of Fig. 1 along lines A-A';

Fig. 3 is a cross sectional view of the memory cell of Fig. 1 along lines B-B';

Figs. 4-10 are cross sectional views of a self-aligned drain contact PMOS flash EPROM process flow according to the present invention;

Fig. 11 is a top view of a PMOS flash memory cell according to the present invention;

Fig. 12 is a cross sectional view of the memory cell of Fig. 11 along lines C-C'; and

Fig. 13 is a cross sectional view of the memory cell of Fig. 11 along lines D-D'.

Use of similar reference numbers in different figures indicates similar or like elements.

DETAILED DESCRIPTION

According to the present invention, a process and structure are provided which allow a reduction in size of flash memory cells by reducing the oxide separation between drain contacts and polysilicon gates through the use of a nitride layer. Figs. 4-10 are side views illustrating a process flow for forming self-aligned drain contacts in flash EPROM cells according to one embodiment of this invention. In Fig. 4, using

conventional methods, a tunnel oxide layer 410 is first formed on a silicon substrate or well 400. A first layer of polysilicon (Poly1) 420, which will later form floating gates for the memory array, is then deposited on tunnel oxide 410. Next, an interpoly dielectric layer 430 is formed on Poly1 420. For example, dielectric layer 430 can be an oxide-nitride-oxide (ONO) layer formed by growing or depositing a layer of silicon dioxide on Poly1 420, followed by depositing a layer of silicon nitride or other suitable insulating nitride and then growing or depositing another layer of silicon dioxide. A second layer of polysilicon (Poly2) 440 or a layer of polycide is then deposited on dielectric layer 430, where Poly2 440 will eventually form the control gates for the memory array. Another layer of silicon dioxide 450 is formed on Poly2 440, followed by a layer of silicon nitride (Nitride1) 460 formed on silicon dioxide layer 450. Silicon dioxide 450 provides padding between Poly2 440 and Nitride1 460. The ranges and preferred thicknesses of these layers are provided in Table 1 below.

Using conventional stacked-gate masking and etching techniques to etch layers 410-460, stacked-gate structures 500 can be formed, as shown in Fig. 5. In Fig. 6, a layer of silicon dioxide (not shown) is first thermally grown on the polysilicon sidewalls of the stacked-gate structures, followed by deposition of another layer of silicon dioxide 610 over the surface of the structure. Because this deposited silicon dioxide layer conforms to the top surface of the structure shown in Fig. 5, a blanket etch, i.e., an oxide etch without a photomask, removes the thinner horizontal portions of this conformal silicon dioxide layer, but leaves the thicker vertical portions of this conformal silicon dioxide layer to form oxide spacers 610 on the vertical sidewalls of stacked-gate

structures 500. A second layer of silicon nitride (Nitride2) 620 is subsequently deposited as a conformal layer and etched isotropically, thereby forming nitride spacers 710 in Fig. 7, which protect the stacked-gate edges during a later drain contact etch.

If desired, a conventional self-aligned source (SAS) etch (not shown for simplicity) may now be performed to decrease the size of the to-be-formed source regions. Referring to Fig. 1, prior to source/drain implantation, field oxide 150b is etched away, which exposes the silicon substrate underneath where dopant implantation for source regions is to occur. The SAS etch aligns floating gate 130 and control gate 140 with the source doping region, thereby eliminating the need for field oxide region 150b to separate the polysilicon gates 130 and 140 from the source region. Dopants can then be implanted during a subsequent step to form source regions 800a and 800b, as shown in Fig. 11. As a result, source region 160b (Fig. 1) is no longer necessary since source region 800b can now connect the source regions from adjacent memory cells.

Thus, an SAS etch is used as a method to reduce source regions, which reduces overall cell size, during a flash EPROM process flow by etching away unnecessary field oxide. The self-alignment of source regions allows closer placement of polysilicon gates, thereby requiring less physical separation between (i.e, allowing closer placement of) one memory cell to the next memory cell.

Regardless of whether an SAS etch is performed, the process flow then continues according to conventional steps. In Fig. 8, P+ regions for the sources 800 and drains 810 are formed, for example, by ion implanting dopants to form source and drain regions and then annealing the resulting structure at 800°C for

20-40 minutes. A layer of boron-phosphorous doped TEOS (BPTEOS) 820 or other suitable dielectric such as BPSG is deposited and smoothed using a reflow process at 850°C for 15-20 minutes. Chemical/mechanical polishing (CMP) is then performed to planarize and reduce BPSG layer 820 down to a thickness of 3000-3500 Å. Table 1 below lists the ranges and preferred values of these various layers.

Layer	Range	Preferred
Tunnel oxide 410	95-105 Å	100 Å
Poly1 420	1000-1500 Å	1200 Å
Dielectric 430	170-200 Å	180 Å
Poly2/Polycide 440	1500-2000 Å	1700 Å
Silicon dioxide 450	250-400 Å	300 Å
Nitride1 460	2500-3000 Å	2700 Å
Sidewall oxide growth	150-200 Å	200 Å
Oxide deposition 610	600-1000 Å	800 Å
Nitride2 620	1000-1200 Å	1000 Å
BPSG (deposited) 820	7000-10000 Å	9000 Å
BPSG (after CMP) 820	3000-3500 Å	3200 Å

Table 1

Conventional masking or direct write techniques can then be used to define drain contact regions. For example, in Fig. 9, after a layer of photoresist (not shown) is deposited on BPSG layer 820, the photoresist is masked to define drain contact region 910. A self-aligned contact etch or high selectivity oxide-to-nitride etch then removes the desired areas of BPSG to form drain contact regions 910. After titanium (Ti) is deposited to form a 400 Å thick layer 920 and titanium nitride (TiN) is deposited to form a 1000 Å thick layer 930 on Ti layer 920, both Ti and TiN are annealed at 585°C for 20 minutes in N_2 to form barrier layers for

deposition of tungsten (W) plugs. In Fig. 10, a 6000 Å thick tungsten layer is deposited into the drain contact region in a well known manner, for example using chemical vapor deposition (CVD). Self-aligned drain contacts 1010 are then formed after CMP or another suitable etchback method planarizes the tungsten layer into tungsten plugs 1020.

Figs. 11-13 show different views of one of stacked gate memory cells 500 formed in accordance with this invention. Fig. 11 is a top view of cell 500 showing drain contact 1010, P+ drain 810, P+ sources 800a and 800b, field oxide 1100, floating gate 420, and control gate 440. Figs. 12 and 13 are cross sectional views of memory cell 500 along lines C-C' and D-D', respectively, of Fig. 11. As seen from Figs. 11 and 12, the size of memory cell 500 is reduced in both the source and the drain regions as compared with memory cell 100 of Figs. 1 and 2. Source regions are reduced by removing field oxide 150b between source 160b and polysilicon gates 130 and 140 in Fig. 1 through a conventional SAS etch. In the present invention, drain regions are reduced because drain contacts can be formed much closer to the polysilicon gates, thereby substantially reducing the amount of oxide between the polysilicon gates and the drain contacts. The result is a much smaller memory cell, which leads to denser memory arrays. The additional oxide, which was needed for possible misalignment of drain contact masks, is eliminated because nitride spacers formed around the polysilicon gates prevent the oxide etch from removing portions of the polysilicon gates. As a result, the stacked-gate etch can be performed to allow more stacked-gate structures 500 to be formed on substrate 400 by reducing the amount of space between each stacked-gate structure 500, as shown in Fig. 5. Furthermore, the drain contact etch can now be

performed without preserving the additional oxide needed to protect the polysilicon gates, which greatly decreases the separation between successive memory cells 500, as shown in Fig. 9. Therefore, using the self-aligned drain contact flow process according to this invention, smaller memory cell sizes and higher density memory arrays are possible.

The above-described embodiments of the present invention are merely meant to be illustrative and not limiting. It will thus be obvious to those skilled in the art that various changes and modifications may be made without departing from this invention in its broader aspects. Therefore, the appended claims encompass all such changes and modifications as fall within the true spirit and scope of this invention.

CLAIMS

We claim:

1. A self-aligned drain contact process flow comprising the steps of:

forming a silicon nitride layer over at least two opposite sides of the stacked-gate portions of to-be-formed memory cells on a silicon substrate;

etching said silicon nitride layer to form nitride spacers on the sides of said stacked gate structures adjacent to-be-formed source and drain regions;

forming source and drain regions in the silicon substrate on opposite sides of each stacked gate structure; and

forming self-aligned drain contacts in select portions of said silicon substrate between said nitride spacers.

2. The process flow of Claim 1, wherein said memory cells are EPROM cells.

3. The process flow of Claim 1, wherein said memory cells are flash EPROM cells.

4. The process flow of Claim 1, wherein said memory cells are PMOS flash EPROM cells.

5. The process flow of Claim 1, wherein said stacked-gate portions of said to-be-formed memory cells are formed comprising the steps of:

forming a first oxide layer on said silicon substrate;

forming a first polysilicon layer on said oxide layer;

forming an interpoly dielectric layer on said first polysilicon layer;

forming a second polysilicon layer on said interpoly dielectric layer;

forming a second oxide layer on said second polysilicon layer;

forming a second silicon nitride layer on said second oxide layer; and

etching said second silicon nitride layer, said first and second oxide layers, said first and second polysilicon layers, and said interpoly dielectric layer.

6. The process of Claim 1, further comprising the step of forming a silicon dioxide layer over at least two opposite sides of said stacked-gate memory cells prior to forming said silicon nitride layer.

7. The process of Claim 6, wherein said silicon dioxide layer is formed comprising the steps of growing and depositing silicon dioxide.

8. The process of Claim 1, wherein said step of forming self-aligned drain contacts comprises the steps of:

depositing a dielectric after said step of forming source and drain regions;

masking selected portions of said dielectric layer to expose drain contact regions;

etching portions of said dielectric layer to uncover said drain contact regions; and

forming conductive plugs in said drain contact regions.

9. The process of Claim 8, wherein said plugs are formed by tungsten deposition.

10. A self-aligned drain contact process flow comprising the steps of:

forming a polysilicon layer over an oxide layer overlying a silicon substrate;

forming a silicon dioxide layer over said polysilicon layer;

forming a silicon nitride layer over said silicon dioxide layer;

etching said silicon nitride, silicon dioxide, polysilicon, and oxide layers to form memory structures;

forming a second silicon dioxide layer over said memory structures;

etching said second silicon dioxide layer to form oxide spacers;

forming a second silicon nitride layer over said second silicon dioxide layer;

etching said second silicon nitride layer to form silicon nitride spacers; and

forming self-aligned drain regions in select portions of said silicon substrate between said silicon nitride spacers.

11. A memory array comprising:

a silicon substrate;

a plurality of alternating drain and source regions formed in said silicon substrate, wherein regions located therebetween define channel regions;

a plurality of memory structures located over said channel regions, said memory structures having at least one polysilicon gate;

a plurality of dielectric spacers located over the sidewalls of said memory structures; and

a plurality of drain contacts located over said drain regions and separated by said

dielectric spacers from the gates in said memory structures.

12. The memory array of Claim 11, further comprising a silicon dioxide layer located between the sidewalls of said memory structures and said dielectric spacers.

13. The memory array of Claim 11, wherein said memory structures comprise:

an oxide located over said channel regions;

a polysilicon floating gate located over said oxide;

an interpoly dielectric located over said floating gate;

a polysilicon control gate located over said interpoly dielectric;

a silicon dioxide layer located over said control gate; and

a silicon nitride layer located over said silicon dioxide layer.

14. The memory array of Claim 11, wherein said memory array is an EPROM array.

15. The memory array of Claim 11, wherein said memory array is a flash EPROM array.

16. The memory array of Claim 11, wherein said memory array is a PMOS flash EPROM array.

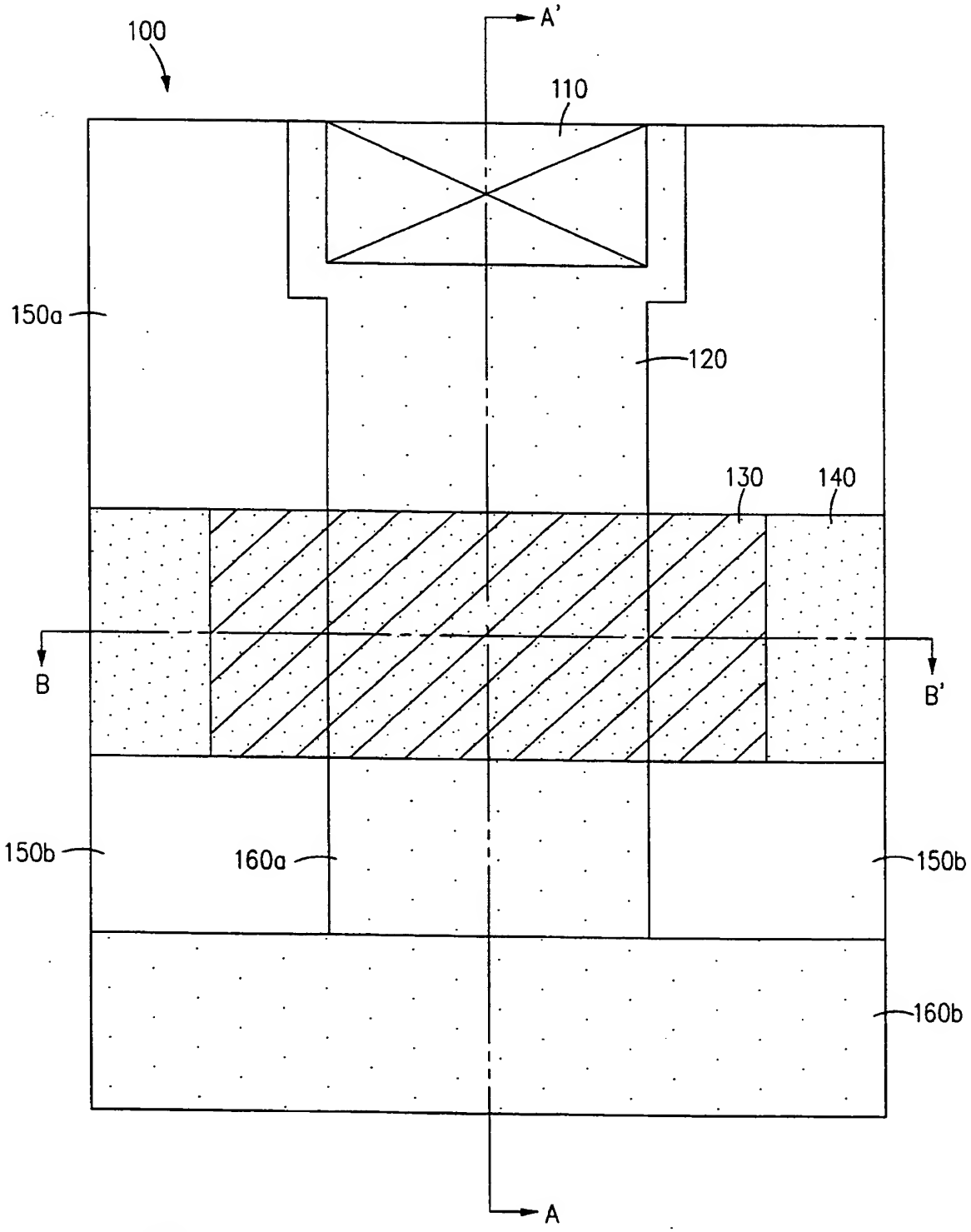
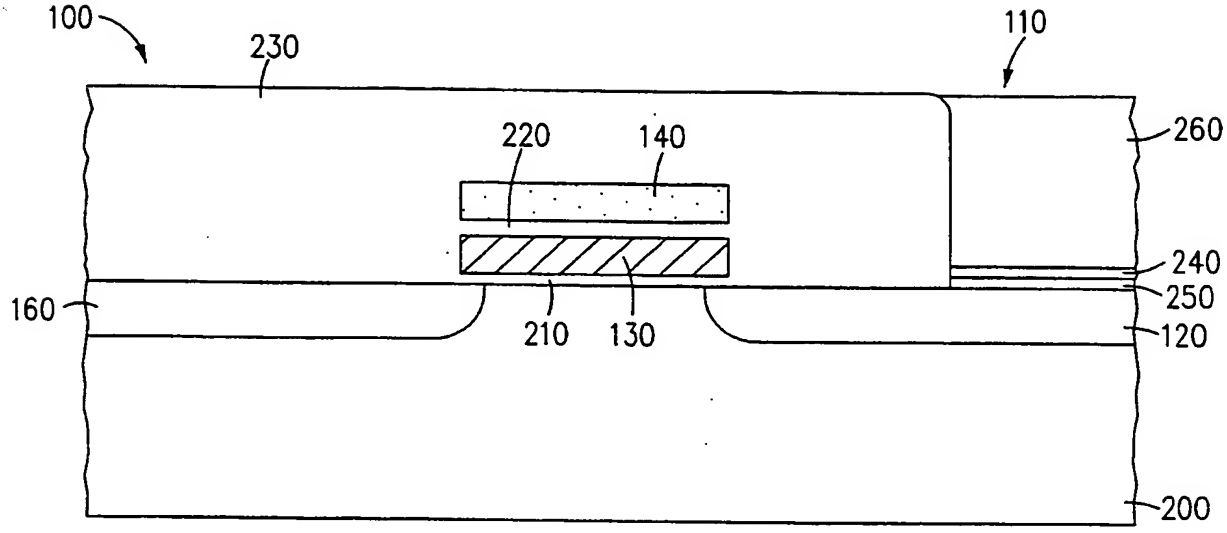


FIG. 1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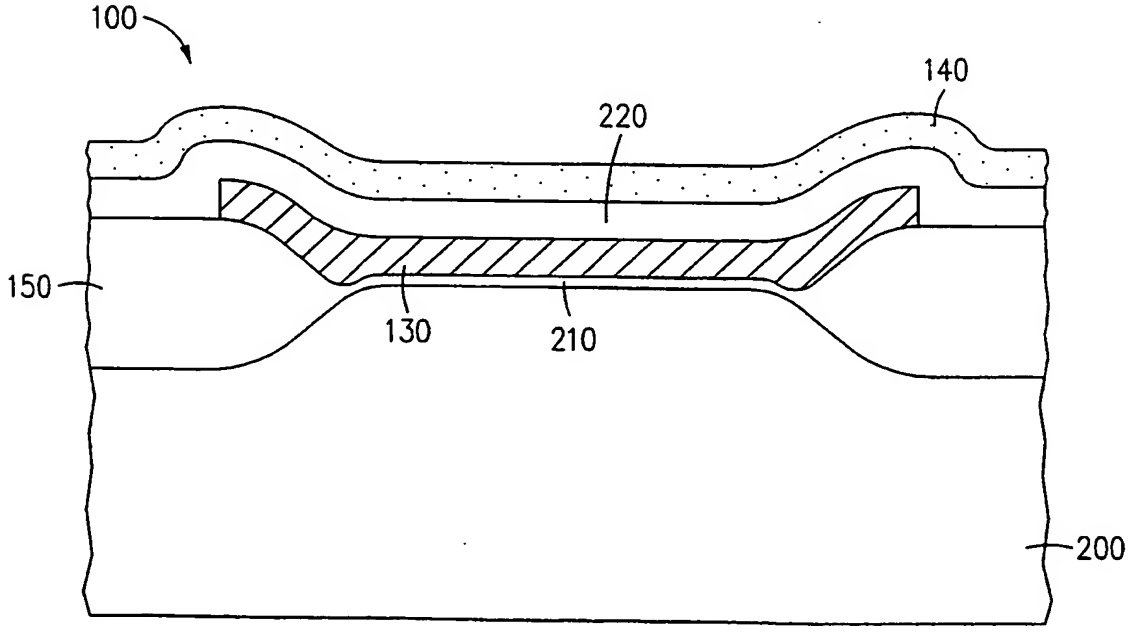
120
200

FIG. 2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130
210
200

FIG. 3

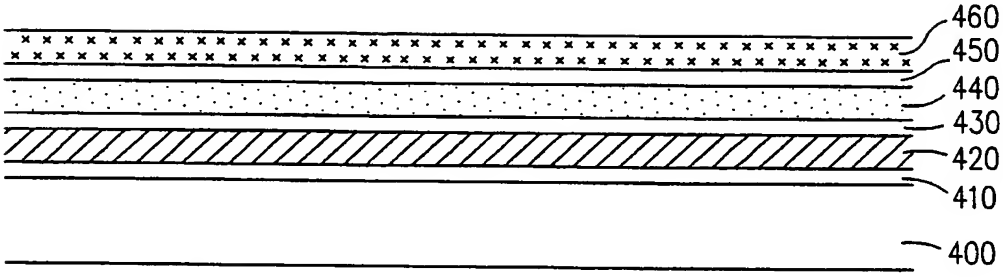


FIG. 4

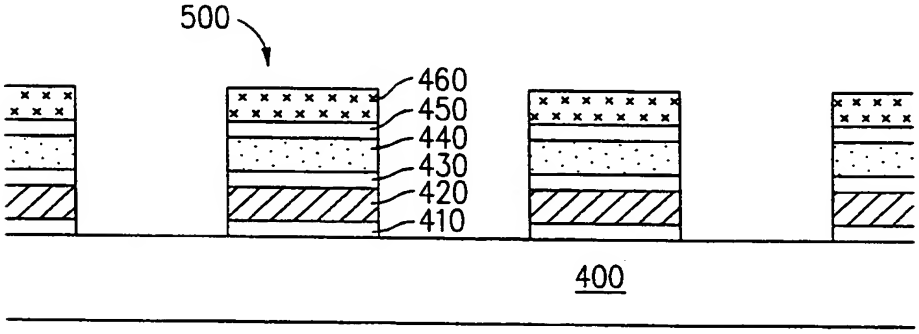


FIG. 5

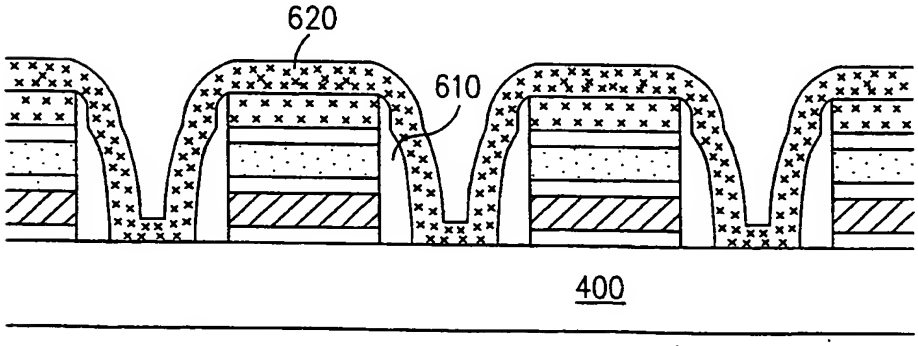


FIG. 6

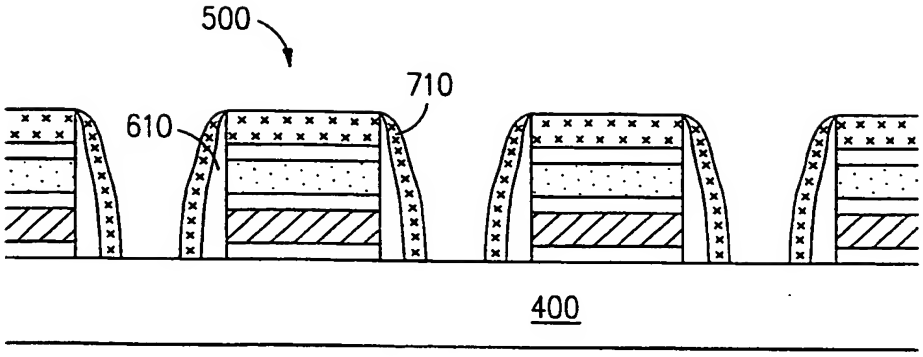


FIG. 7

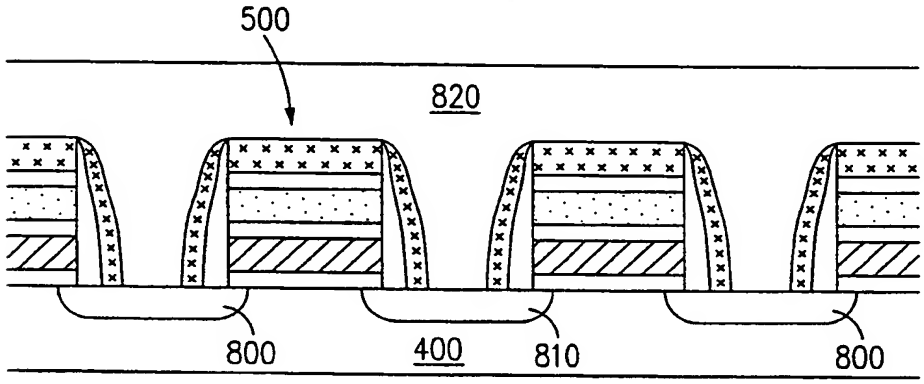


FIG. 8

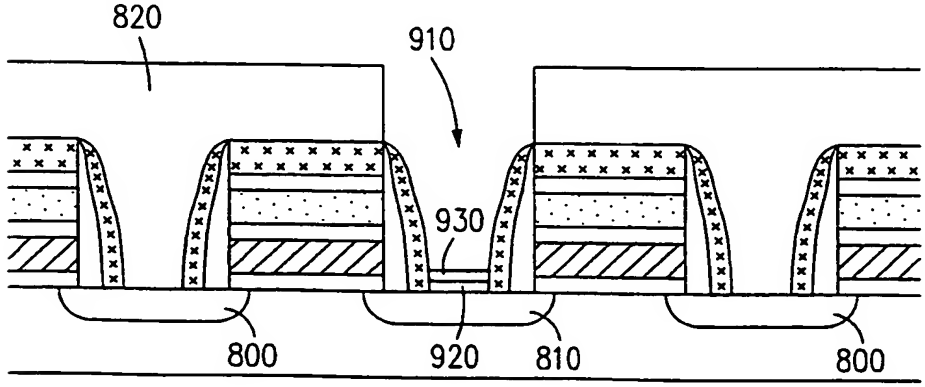


FIG. 9

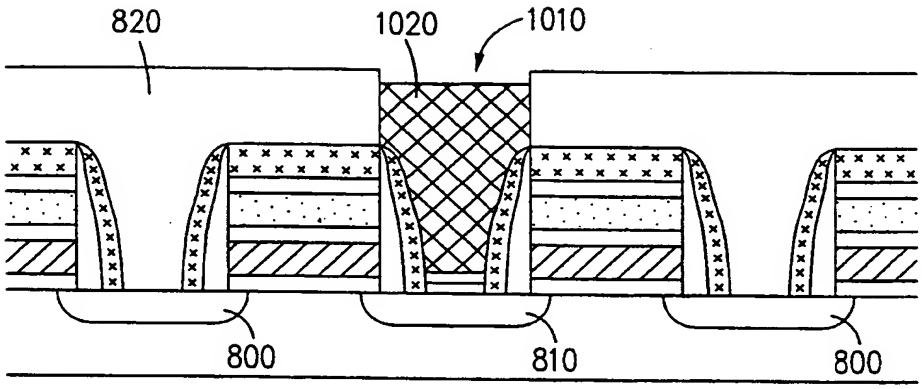
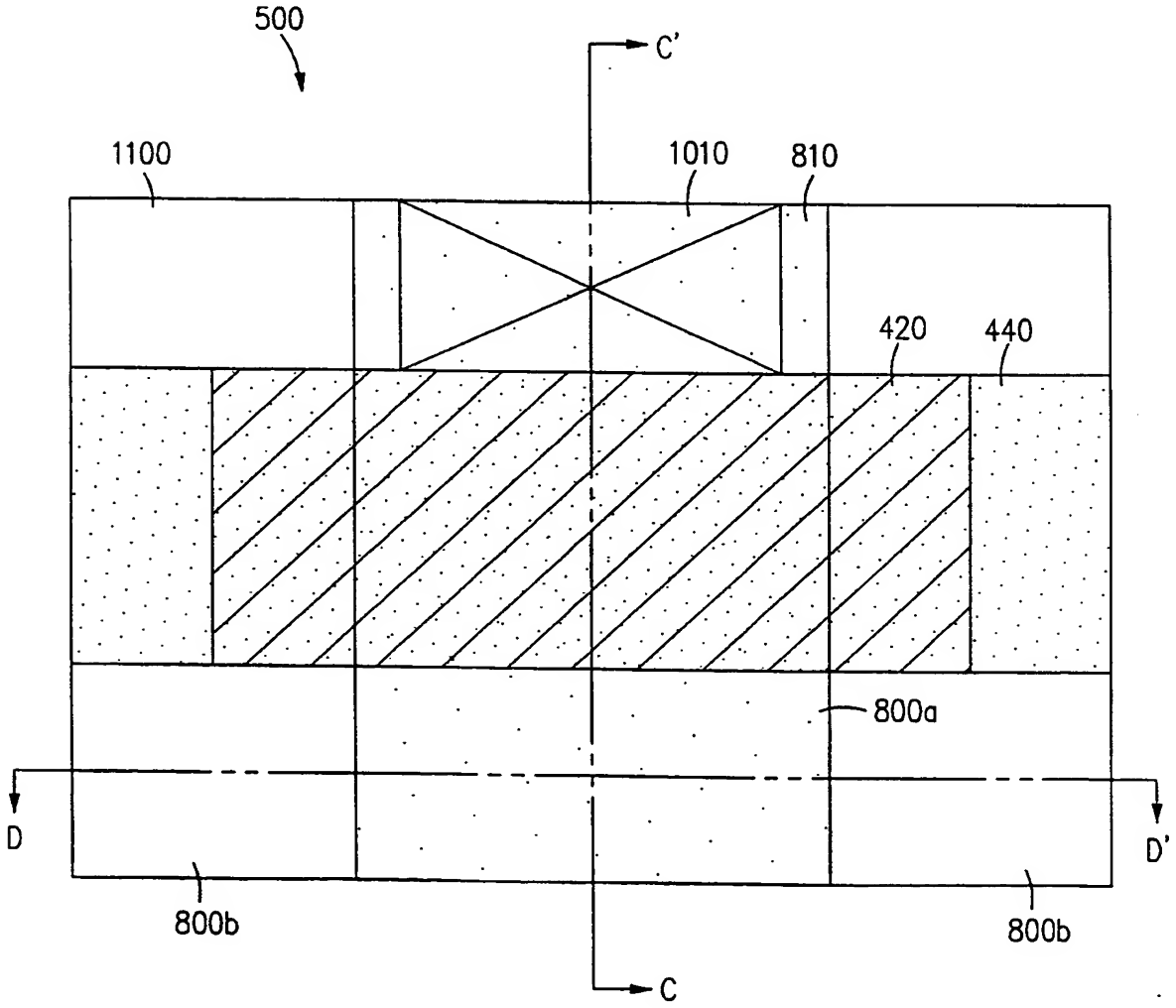

820
1020
1010
800
810
800

FIG. 10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C'
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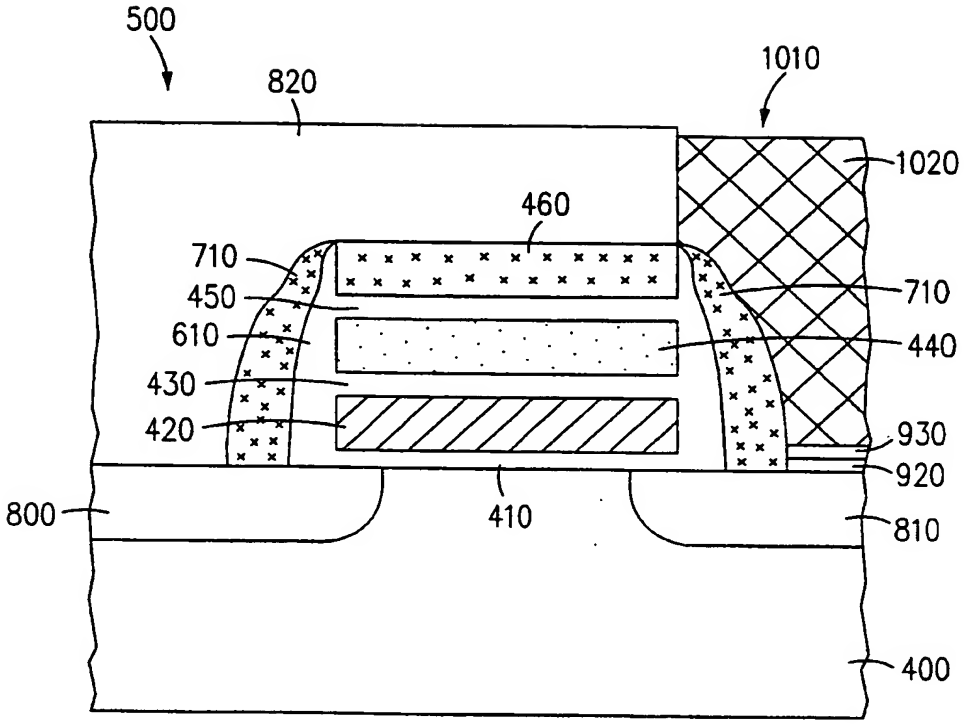
420
440
800a
D
D'
800b
800b
C

FIG. 11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820
1010
1020
460
710
450
610
430
420
710
440
930
920
800
410
810
400

FIG. 12

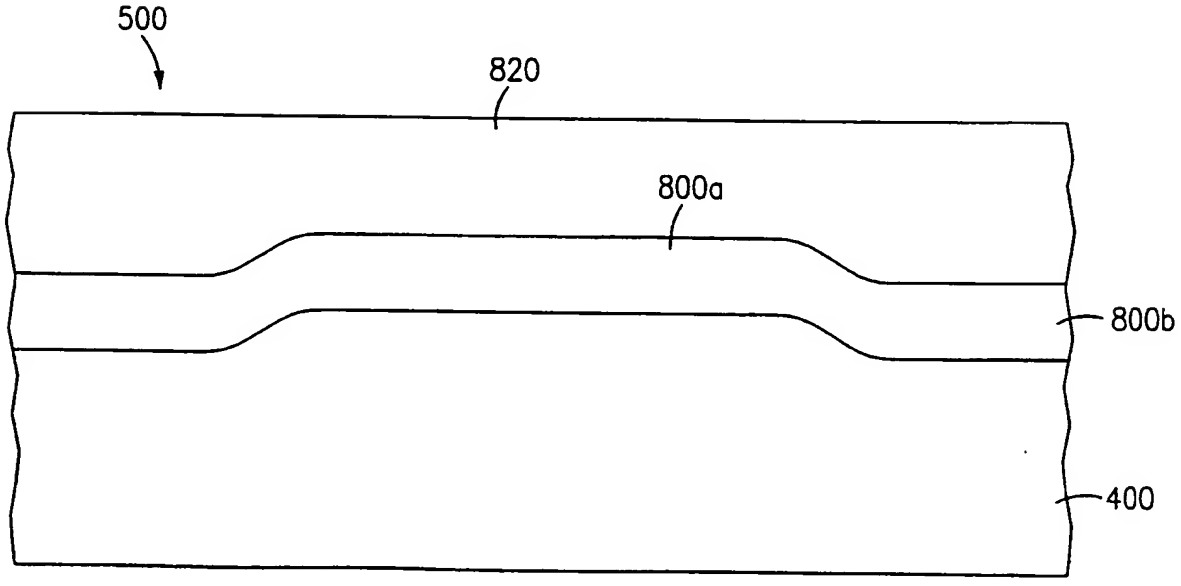
500
820
800a
800b
400

FIG. 13

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 98/02977

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/8247 H01L27/115

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 631 179 A (SUNG HUNG-CHENG ET AL) 20 May 1997 see the whole document	1-16
X	FR 2 711 275 A (INTEL CORP) 21 April 1995 see the whole document	1-16
X A	US 5 661 054 A (LEE ROGER ET AL) 26 August 1997 see the whole document	1-5,8,9, 11,13-16 6,7,10
A	US 5 270 240 A (LEE ROGER R) 14 December 1993 see the whole document	1-16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
15 January 1999	21/01/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Albrecht, C

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/US 98/02977

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5631179 A	20-05-1997	US 5814862 A	29-09-1998
FR 2711275 A	21-04-1995	JP 7169866 A	04-07-1995
		US 5731242 A	24-03-1998
US 5661054 A	26-08-1997	US 5736444 A	07-04-1998
		US 5751039 A	12-05-1998
US 5270240 A	14-12-1993	US 5149665 A	22-09-1992

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